

2.7V to 30V Input 55µA Quiescent Current Synchronous Boost Controller

Description

The MT5086 is a high efficiency synchronous Boost PWM controller that drives all N-channel power MOSFETs to step up output voltage up to 30V. Synchronous rectification increases efficiency, reduces power losses and eases thermal requirements, allowing the MT5086 to be used in high power step-up applications. The 2.7V to 30V input voltage range supports a wide range of battery and AC powered inputs. The 55µA no load quiescent current extends operating run time in battery-powered systems.

The adjustable operating frequency (100kHz to 1MHz) can be synchronized to an external clock with the internal PLL. The MT5086 also features a precision 1.203V reference and a power good output indicator. The MODE/SYNC pin selects between pulse skipping mode and forced PWM mode at light loads.

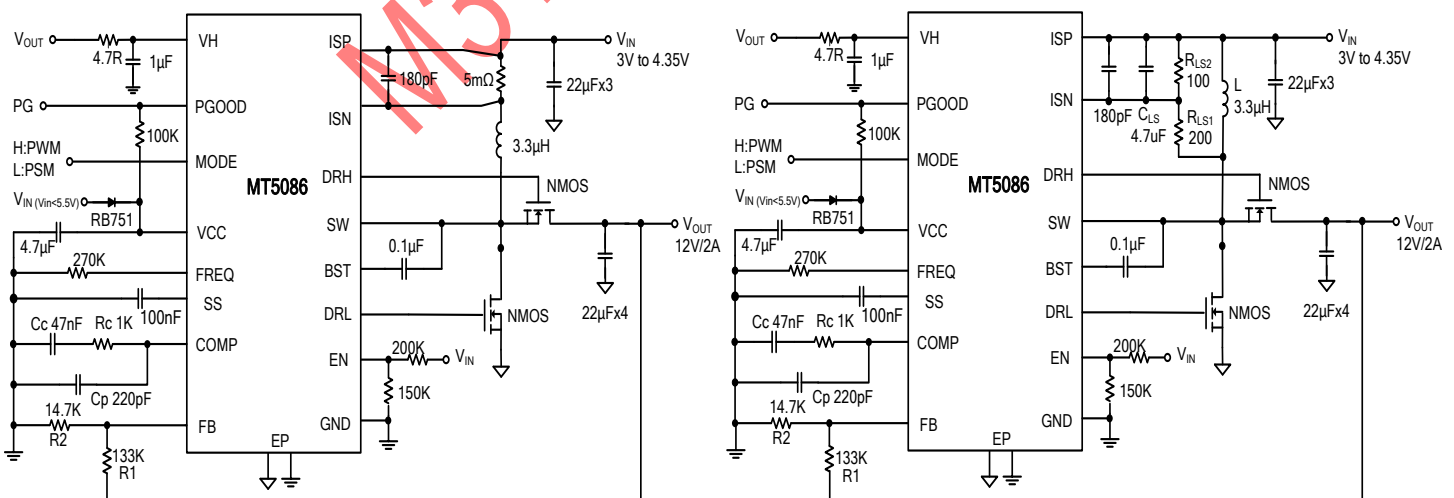
Features

- 2.7V to 30V (40V ABS Max) Input Range
- 3V to 30V Programmable Output Voltage
- ±1.5% 1.203V Reference Voltage
- Low Quiescent Current 55µA
- Low 5µA Shutdown Supply Current
- Adjustable Input UVLO through EN pin
- Resistor or Inductor DCR Current Sensing
- Adjustable Frequency from 100kHz to 1MHz with Synchronization Capability to an external clock
- Output Voltage Power Good Indicator
- Internal 5.4V LDO for Gate Drive Supply
- Cycle-by-Cycle Current Limit
- Thermal Shutdown
- QFN3mmx3mm\_16L Packages
- Pb-Free ROHS compliant

Application

- 5V, 9V, 12V, 20V and 24 VDC Bus Power
- Power Banks and Electronic Cigarette
- USB-PD and Thunderbolt Ports for PCs
- Tablet Computer Accessories
- Industrial Battery Powered Systems
- RF Power Amplifiers
- Synchronous Flyback

Typical Application



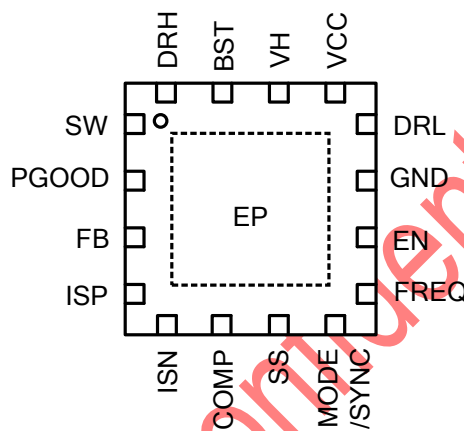
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**Ordering Information**

Part No.	Marking	Temp. Range	Package	MOQ
MT5086NQAR	MT5086 YWWXX	-40°C ~+85°C	QFN3x3_16L	5,000/Reel

Note: Y: Year, WW: Week, XX: Control Code

**Pin Configuration**



**MT5086 TOP VIEW**

**Pin Description**

PIN NAME	PIN NO.	DESCRIPTION
SW	1	Switching node of the Step-up converter. Connect this pin to the drain of the low side MOSFET, the source of high side synchronous MOSFET and the inductor.
PGOOD	2	Power Good Indicator. Open-drain output that is pulled to ground when the output voltage is more than ±10% away from the regulated output voltage. A 100kΩ pull-up resistor is recommended between PGOOD and VCC.
FB	3	Error amplifier input and feedback pin for voltage regulation. Connect FB to the center tap of a resistor divider to set the output voltage.
ISP	4	Positive Current Sense Amplifier Input. The current sense resistor is normally placed at the input of the step-up controller in series with the inductor.
ISN	5	Negative Current Sense Amplifier Input. The common mode voltage range on the ISP and ISN pins is 2.5V to 30V (40V ABS Max).
COMP	6	Output of the internal transconductance error amplifier. The feedback loop compensation network is connected from COMP pin to GND.

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PIN NAME	PIN NO.	DESCRIPTION
SS	7	Soft-start programming pin. An external capacitor sets the ramp rate of the output voltage during soft-start period. Recommend to place a 0.1 $\mu$ F ceramic capacitor from SS to GND for the most applications.
MODE /SYNC	8	Light Load Pulse-skip mode or Forced-PWM mode control and an external clock synchronization input. An internal 100k resistor to GND sets automatically pulse-skip mode at light load condition when the pin is floated. There are three operating modes: <ul style="list-style-type: none"> <li>• MODE/SYNC low or Float: Operate in pulse-skip mode at light load.</li> <li>• MODE/SYNC high: Operate in force-PWM mode at light load with the oscillator frequency set at FREQ pin by R<sub>FREQ</sub>.</li> <li>• MODE/SYNC clocked: Operate in force-PWM mode at light load with the oscillator frequency set by SYNC clock input. Force the rising DRL signal to be synchronized with the rising edge of the external clock.</li> </ul>
FREQ	9	Oscillator Frequency Set Input. A resistor from FREQ to GND sets the oscillator from 100kHz to 1000kHz (Typical R <sub>FREQ</sub> =220k $\Omega$ sets Fosc=300kHz). R <sub>FREQ</sub> is still required if an external clock is used at MODE/SYNC pin.
EN	10	Enable input. Pull EN above 1.205V to turn on the converter and pull EN below 1.10V to shut down the converter. EN pin can be used to implement adjustable input voltage under voltage lockout (UVLO) using two resistors. Connect EN to the center tap of a resistor divider to set the input UVLO threshold.
GND	11	Ground pin. Connect this pin to the source of the bottom (main) N-channel MOSFET and the (-) terminal(s) of C <sub>IN</sub> and C <sub>OUT</sub> . All small-signal components and compensation components should also connect to this ground.
DRL	12	Low side gate driver output. Connect this pin to the gate of the low side N-channel MOSFET. When VH bias is removed, an internal 200k $\Omega$ resistor pulls DRL to GND.
VCC	13	5.4V On-Chip Low Dropout Linear Regulator Output (LDO). This regulator powers all internal circuitry including the low side and high side N-channel MOSFET gate drivers. Bypass VCC to GND with a 1 $\mu$ F or greater ceramic capacitor. <b><u>When the input voltage VIN is &lt; 3.5V, Connect VCC to VIN through a Diode.</u></b>
VH	14	The supply pin to On-Chip LDO Regulator. The operating voltage range on this pin is 2.7V to 30V (40V abs max). Bypass VH to GND with a 0.1 $\mu$ F ceramic capacitor. <b><u>When the input voltage VIN is &lt; 5.5V, connect VH to the output VOUT of step-up converter to get maximum voltage for gate drivers.</u></b> <b><u>When the input voltage Vin is &gt; 5.5V, connect VH to the Vin input voltage to improve efficiency.</u></b>
BST	15	Bootstrap capacitor node for high-side MOSFET gate driver. Connect the bootstrap capacitor 0.1 $\mu$ F from this pin to the SW pin.
DRH	16	High side gate driver output. Connect this pin to the gate of the high side synchronous rectifier N-channel MOSFET.
EP	EP	Exposed pad must be soldered to achieve appropriate power dissipation. Connect EP to GND.